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Xilinx 公司及产品介绍 2017.4

XILINX
ALL PROGRAMMABLE.

Xilinx: All Programmable

软件定义 | 硬件优化

或许您了解 Xilinx 是因为我们创造了 FPGA，也或许您知道我们是因为我们发明 FPGA 颠覆了半导体世界，还可能是因为我们创立了 Fabless（无晶圆厂）的半导体模式。我们拥有超过 3500 项专利和超过 60 个行业第一，我们基于“客户第一”的原则持续不断地开拓新的可编程技术。今天，Xilinx 的产品组合融合了 FPGA、SoC 和 3DIC 系列 All Programmable 器件，以及全可编程的开发模型，包括软件定义的开发环境等。我们的产品支持 5G 无线、嵌入式视觉、工业物联网和云计算所驱动的各种智能、互连和差异化应用。

嵌入式视觉 • 工业物联网 • 云计算 • 5G 无线

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文档提醒

当产品变更/停用通知以及设计咨询答复记录等产品文档发布时，

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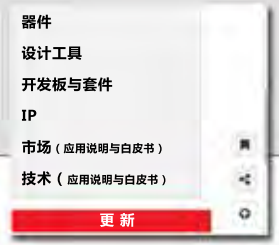

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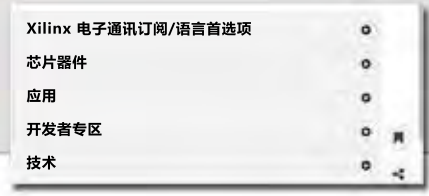

书签

您可以保存任何网页，以便以后轻松恢复。

技术支持

打开服务申请，联系 Xilinx 专家。通过设计过程的每个步骤获得有关产品使用及故障诊断的帮助。

轻松打造响应最快且可重配置的视觉系统

reVISION
Responsive and Reconfigurable Vision Systems

响应最快且可重配置的视觉系统

领先的系统开发商正在新一代视觉导向机器学习系统中使用全可编程系统。为加速生产力，Xilinx 已面向软硬件及系统开发人员创建了集聚实用资源的 reVISION 专区。

此外，我们还面向希望分享其参考设计、库和经验的开发人员，提供了一个有各种社区项目的空间。

立即访问该专区，然后开始构建响应最快且可重配置的视觉导向系统。

reVISION简介　计算机视觉　机器学习　连接与传感器支持　设计范例

reVISION 可实现响应最快且可重配置的视觉系统

比一般 SoC 及嵌入式 GPU 响应性更高：

在机器学习中，每秒每瓦图像提升 6 倍

计算机视觉处理，每秒每瓦帧数提升 42 倍

时延仅为 1/5

可重新配置为最新的算法和传感器：

不断升级至最新的机器学习算法

支持最新传感器类型及连接标准

支持高达 8K 的分辨率及自定义分辨率

软件定义及更高易用性：

随时可使用 OpenCV 库加速开发

可利用 C/C++ 及 OpenCL 语言的任意组合

可利用 Caffe 等开源机器学习框架进行开发

立即开始利用现有的 Xilinx 及生态系统设计硬件、模块和生产就绪型系统级模块 (SOM)，围绕 Zynq SoC/MPSoC 及 FPGA 设计您的计算机视觉系统。

第一时间了解 reVISION 背景资料、白皮书及视频演示信息。敬请扫描二维码访问：
http://china.xilinx.com/revision

XILINX ALL PROGRAMMABLE™

工业物联网解决方案

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更智能的工厂、城市、医疗和能源

工业物联网 (IIoT) 正在推动第四轮工业革命。 它极大地改变着制造、能源、交通运输、城市、医疗以及其它工业行业。大部分专家认为 IIoT 时代已悄然来到，带来了实实在在可测量的业务影响。

IIoT 可帮助企业从传感器收集、聚集和分析数据，从而可最大限度提高机器效率以及整个工作的吞吐量。应用包括运动控制、机器与机器通信、预测性维护、智能能源/电网、大数据分析以及等智能互联医疗系统等。

Xilinx 提供了面向工业物联网的灵活的标准化解决方案，包括全可编程，实时处理，硬件优化和针对保密和安全的"任意"互联。Xilinx SDAccel™、SDSoC™ 和 Vivado® HLS 可帮助客户快速开发更智能的互连差异化应用。

5 大差异化优势

"精确、预判、保密、安全和互联互通"

1. 传感器融合与分析
2. 任意连接
3. 最高精度的运动控制
4. 可重用的 All Programmable 平台
5. 仅采用单芯片的高度安全和保密的平台

驱动工业物联网：

工厂自动化、医疗、能源、监控、科学

扫我了解更多信息

视频/视觉解决方案

POWERED BY XILINX

更智能的工厂、城市、医疗和能源

嵌入式视觉是当今科技最激动人心的领域之一。Xilinx 将嵌入式视觉看作一个塑造电子技术产业未来的、无处不在的重大趋势。

Xilinx 为嵌入式视觉开发人员提供一系列支持软硬件设计的技术和器件，包括 FPGA、SoC 以及 MPSoC。

Xilinx Vivado HLx 设计环境可帮助硬件及平台开发商开发最新嵌入式视觉硬件。这些工具支持业界最新高带宽传感器接口。Xilinx 包括 SDSoC 在内的 SDx 工具有助于软件及算法开发人员在基于 Eclipse 的熟悉环境中采用 C、C++ 和 OpenCL 等计算机语言进行开发。

Xilinx reVISION 协议栈建立在 SDx 概念基础之上，支持 OpenCV 和机器学习推理，从而支持 AlexNet、GoogLeNet、SqueezeNet、SSD 和 FCN 等最普及的神经网络以及构建定制神经网络 (CNN/DNN) 所需的功能元件。同时，该协议栈还允许设计团队将预定义的优化 CNN 实现方案用于网络层。这得到了加速型 OpenCV 函数的有力补充，支持计算机视觉处理。

5 大差异化优势

"精确的视觉"

1. 实时图像识别与分析
2. All Programmable 平台的复用优势
3. 可扩展传感器融合
4. 最高性能功耗比
5. 仅采用单芯片带来的安全性和保密性

驱动嵌入式视觉：

ADAS、机器视觉、监控、无人机、医疗、专业音视频、显示器……

扫我了解更多信息

不断壮大的全可编程 SoC 产品阵营

POWERED BY XILINX

不断壮大的全可编程 SoC 产品阵营

Xilinx 全可编程 SoC 产品系列将处理器的软件可编程性与 FPGA 的硬件可编程性进行完美整合，可为您提供无与伦比的系统性能、灵活性与可扩展性。该产品系列可为您的设计带来更低功耗与更低成本的整体系统优势以及快速上市进程。与传统 SoC 处理解决方案不同，高度灵活的可编程逻辑可为您实现优化和差异化，允许您添加外设与加速器，从而可帮助您适应各种广泛的应用。

Zynq UltraScale+ MPSoC 产品优势

Zynq® UltraScale+™ MPSoC 器件不仅提供 64 位处理器可扩展性，同时还将实时控制与软硬件引擎相结合，支持图形、视频、波形与数据包处理。基于带有通用实时处理器及可编程逻辑的平台，三个不同的子系列包括带有双核应用处理器的 CG 器件，带有四核应用处理器和 GPU 的 EG 器件，以及带有视频编解码器的 EV 器件。它们为 5G 无线通信，下一代 ADAS 和工业物联网应用创造了无限可能性。

处理系统	Zynq-7000 SoC	Zynq UltraScale+ MPSoC
应用处理单元	Single/Dual ARM Cortex-A9 MPCore	Dual/Quar ARM Cortex-A53 MPCore
实时处理单元	–	Dual ARM Cortex-R5 MPCore
多媒体处理	–	ARM Mali-400 MP2
动态内存接口	DDR3, DDR3L, DDR2, LPDDR2	DDR4, LPDDR4, DDR3, DDR3L, LPDDR3
高速外设	USB 2.0, Gigabit Ethernet, SD/SDIO	PCIe Gen2, USB 3.0, SATA 3.1, DisplayPort, Gigabit Ethernet, SD/SDIO
安全性	RSA, AES, and SHA, ARM TrustZone	RSA, AES, and SHA, ARM TrustZone
最大 I/O 引脚	128	214

XILINX ALL PROGRAMMABLE™

Zynq UltraScale+ MPSoCs: CG Devices

		Device Name[1]	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Processing System (PS)	Application Processor Unit	Processor Core	**Dual-core** ARM® Cortex™-A53 MPCore™ up to 1.3GHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB						
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore up to 533MHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core						
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC						
		Static Memory Interfaces	NAND, 2x Quad-SPI						
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet						
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains						
		Security	RSA, AES, and SHA						
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor						
PS to PL Interface			12 x 32/64/128b AXI Ports						
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600
		CLB Flip-Flops (K)	94	141	176	234	429	461	548
		CLB LUTs (K)	47	71	88	117	215	230	274
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
		UltraRAM (Mb)	-	-	14.0	18.0	-	27.0	-
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4
	Integrated IP	DSP Slices	240	360	728	1,248	1,973	1,728	2,520
		PCI Express® Gen 3x16 / Gen4x8	-	-	2	2	-	2	-
		150G Interlaken	-	-	-	-	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-
		AMS - System Monitor	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	16	16	24	24	24
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-
	Speed Grades	Extended[2]	-1 -2 -2L						
		Industrial	-1 -1L -2						

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (T) = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

Zynq UltraScale+ MPSoCs: EG Devices

	Device Name[1]	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz									
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB									
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz									
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core									
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz									
		Memory	L2 Cache 64KB									
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC									
		Static Memory Interfaces	NAND, 2x Quad-SPI									
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet									
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains									
		Security	RSA, AES, and SHA									
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor									
PS to PL Interface			12 x 32/64/128b AXI Ports									
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	94	141	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	47	71	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	14.0	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express® Gen 3x16 / Gen4x8	-	-	2	2	-	2	-	4	-	4	5
		150G Interlaken	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[2]	-1 -2 -2L			-1 -2 -2L -3				-1 -2 -2L -3			
		Industrial	-1 -1L -2										

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (T_j = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

Zynq UltraScale+ MPSoCs: EV Devices

		Device Name[1]	ZU4EV	ZU5EV	ZU7EV
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB		
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core		
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz		
		Memory	L2 Cache 64KB		
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC		
		Static Memory Interfaces	NAND, 2x Quad-SPI		
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet		
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains		
		Security	RSA, AES, and SHA		
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor		
PS to PL Interface			12 x 32/64/128b AXI Ports		
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	192	256	504
		CLB Flip-Flops (K)	176	234	461
		CLB LUTs (K)	88	117	230
	Memory	Max. Distributed RAM (Mb)	2.6	3.5	6.2
		Total Block RAM (Mb)	4.5	5.1	11.0
		UltraRAM (Mb)	14.0	18.0	27.0
	Clocking	Clock Management Tiles (CMTs)	4	4	8
	Integrated IP	DSP Slices	728	1,248	1,728
		Video Codec Unit (VCU)	1	1	1
		PCI Express® Gen 3x16 / Gen4x8	2	2	2
		150G Interlaken	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-
		AMS - System Monitor	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	16	16	24
		GTY 32.75Gb/s Transceivers	-	-	-
	Speed Grades	Extended[2]	-1 -2 -2L -3		
		Industrial	-1 -1L -2		

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (T_j = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

Zynq UltraScale+ MPSoCs

PS I/Os[1], 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os
PS-GTR 6Gb/s, GTH 16.3Gb/s, GTY 32.75Gb/s

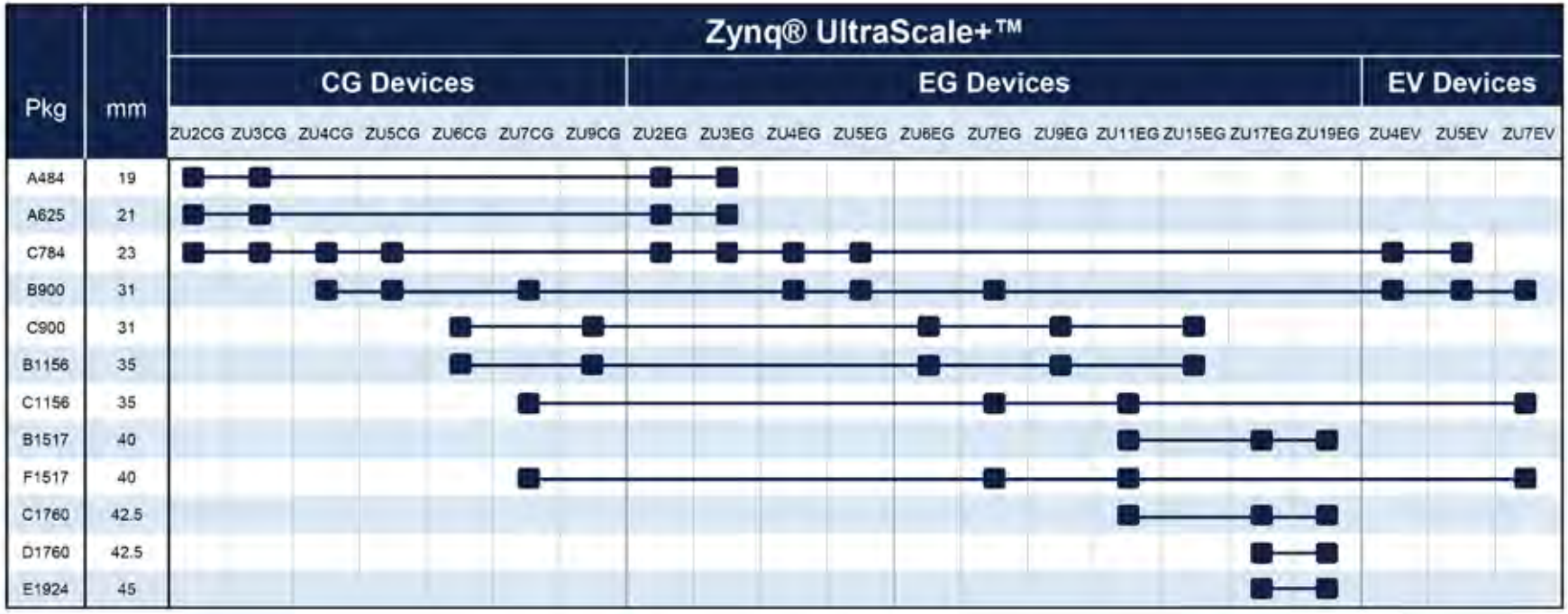
Pkg Footprint[2,3]	Dimensions (mm)	ZU2	ZU3	ZU4	ZU5	ZU6	ZU7	ZU9	ZU11	ZU15	ZU17	ZU19
A484[4]	19x19	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0									
A625[4]	21x21	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0									
C784[4,5]	23x23	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
B900	31x31			214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0					
C900	31x31					214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		
B1156	35x35					214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		
C1156	35x35						214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0			
B1517	40x40								214, 72, 416 4, 16, 0		214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
F1517	40x40						214, 48, 416 4, 24, 0		214, 48, 416 4, 32, 0			
C1760	42.5x42.5								214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16
D1760	42.5x42.5										214, 48, 260 4, 44, 28	214, 48, 260 4, 44, 28
E1924	45x45										214, 96, 572 4, 44, 0	214, 96, 572 4, 44, 0

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Notes
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence.
3. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
4. These packages are only offered in 0.8mm ballpitch. All other packages are offered in 1.0mm ball pitch.
5. GTH transceivers in the C784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+ MPSoC Device Migration Table

The Zynq UltraScale+ family provides footprint compatibility to enable users to migrate designs from one device to another. Any two packages with the same footprint identifier code (last letter and number sequence) are footprint compatible.



Zynq Ultracale+ MPSOC Ordering Information

Zynq-7000 All Programmable SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM	1.8Mb	2.5Mb	3.8Mb	2.1Mb	3.3Mb	4.9Mb	9.3Mb	17.6Mb	19.1Mb	26.5Mb
	(# 36Kb Blocks)	(50)	(72)	(107)	(60)	(95)	(140)	(265)	(500)	(545)	(755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
	Speed Grades: Commercial	-1			-1			-1			-1
	Speed Grades: Extended	-2			-2,-3			-2,-3			-2
	Speed Grades: Industrial	-1, -2			-1, -2, -1L			-1, -2, -2L			-1, -2, -2L

Notes:
1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. See DS190, *Zynq-7000 All Programmable SoC Overview* for details.
2. Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* for more details.
3. Security block is shared by the Processing System and the Programmable Logic.

Zynq-7000 All Programmable SoC Family

HR I/O, HP I/O, PS I/O, and Transceivers (GTP or GTX)

Package Footprint	Device Name Dimensions (mm)[1]	Cost-Optimized Devices						Mid-Range Devices			
		Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
		HR I/O, HP I/O PS I/O[2], GTP Transceivers						HR I/O, HP I/O PS I/O[2], GTX Transceivers			
CLG225	13x13	54, 0 84[3], 0			54, 0 84[3], 0						
CLG400	17x17	100, 0 128, 0		125, 0 128, 0	100, 0 128, 0		125, 0 128, 0				
CLG484	19x19			200, 0 128, 0			200, 0 128, 0				
CLG485[4]	19x19		150, 0 128, 4			150, 0 128, 4					
SBG485 / SBV485[4]	19x19							50, 100 128, 4			
FBG484 / FBV484	23x23							100, 63 128, 4			
FBG676 / FBV676[1]	27x27							100, 150 128, 4	100, 150 128, 8	100, 150 128, 8	
FFG676 / FFV676[1]	27x27							100, 150 128, 4	100, 150 128, 8	100, 150 128, 8	
FFG900 / FFV900	31x31								212, 150 128, 16	212, 150 128, 16	212, 150 128, 16
FFG1156 / FFV1156	35x35										250, 150 128, 16

Notes:
1. Devices in the same package are footprint compatible. FBG676 / FBV676 and FFG676 / FFV676 are also footprint compatible.
2. PS I/O count does not include dedicated DDR calibration pins.
3. PS DDR and PS MIO pin count is limited by package size. See DS190, *Zynq-7000 All Programmable SoC Overview* for details.
4. CLG485 and SBG485 / SBV485 are pin-to-pin compatible. See product data sheets and user guides for more details. See DS190, *Zynq-7000 All Programmable SoC Overview* for package details.

Zynq-7000 Device Ordering Information

Footprint

XC	7	Z	###	S	-1	FF	V	###	C
Xilinx Commercial	Series	Zynq	Value Index	Single Core Indicator (Z-7007S Z-7012S Z-7014S only)	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest	CL: Wire-bond Molded (.8mm) SB: Flip-chip Lidless (.8mm) FB: Flip-chip Lidless (1mm) FF: Flip-chip Lidded (1mm)	V: RoHS 6/6 G (CLG) = RoHS 6/6 G (SBG, FBG, FFG) = RoHS 6/6 with exemption 15	Package Pin Count	Temperature Grade (C, E, I)

C = Commercial (Tj = 0°C to +85°C)
E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = –40°C to +100°C)

Refer to DS190, Zynq-7000 All Programmable SoC Overview for additional information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Kintex UltraScale+ FPGAs

	Device Name	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
Logic	System Logic Cells (K)	356	475	600	653	747	1,143
	CLB Flip-Flops (K)	325	434	548	597	683	1,045
	CLB LUTs (K)	163	217	274	299	341	523
Memory	Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8
	Total Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6
	UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0
Clocking	Clock Mgmt Tiles (CMTs)	4	4	4	8	4	11
Integrated IP	DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968
	PCIe® Gen3 x16 / Gen4 x8	1	1	0	4	0	5
	150G Interlaken	0	0	0	1	0	4
	100G Ethernet w/RS-FEC	0	1	0	2	0	4
I/O	Max. Single-Ended HD I/Os	96	96	96	96	96	96
	Max. Single-Ended HP I/Os	208	208	208	416	208	572
	GTH 16.3Gb/s Transceivers	0	0	28	32	28	44
	GTY 32.75Gb/s Transceivers	16	16	0	20	0	32
Speed Grades	Extended[1]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2

Footprint compatible with 20nm UltraScale Devices with same footprint identifier

Footprint[2, 3]	Dimensions (mm)	HD I/O, HP I/O, GTH 16.3Gb/s, GTY 32.75Gb/s					
B784[4]	23x23[5]	96, 208, 0, 16	96, 208, 0, 16				
A676[4]	27x27	48, 208, 0, 16	48, 208, 0, 16				
B676	27x27	72, 208, 0, 16	72, 208, 0, 16				
D900[4]	31x31	96, 208, 0, 16	96, 208, 0, 16		96, 312, 16, 0		
E900	31x31			96, 208, 28, 0		96, 208, 28, 0	
A1156[4]	35x35				48, 416, 20, 8		48, 468, 20, 8
E1517	40x40				96, 416, 32, 20		96, 416, 32, 24
A1760	42.5x42.5						96, 416, 44, 32
E1760	42.5x42.5						96, 572, 32, 24

Notes:
1. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS890, UltraScale Architecture and Product Overview.
2. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
3. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product* Overview.
4. GTY transceiver line rates are package limited: B784 to 12.5 Gb/s; A676, D900, and A1156 to 16.3 Gb/s. Refer to data sheet for details.
5. The B784 package is only offered in 0.8mm ball pitch. All other packages are 1.0mm ball pitch.

Virtex UltraScale+ FPGAs

Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	962	962	1,907	2,852
CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	879	879	1,743	2,607
CLB LUTs (K)	394	601	788	1,182	1,296	1,728	440	440	872	1,304
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
HBM AXI Interfaces	–	–	–	–	–	–	32	32	32	32
Clock Mgmt Tiles (CMTs)	10	20	20	30	12	16	4	4	8	12
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	8.9	8.9	18.6	28.1
PCIe® Gen3 x16 / Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports[1]	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/ RS-FEC	3	4	6	9	9	12	2	2	5	8
Max. Single-Ended HP I/Os	520	832	832	832	624	832	208	208	416	624
GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	32	32	64	96
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	–	–	–

Footprint compatible with 20nm UltraScale Devices with same footprint identifier

Footprint[3,4]	Dimensions (mm)	HP I/O, GTY 32.75Gb/s								
C1517	40x40	520, 40								
F1924[5]	45x45					624, 64				
A2104	47.5x47.5		832, 52	832, 52	832, 52					
	52.5x52.5[6]						832, 52			
B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76				
	52.5x52.5[6]						702, 76			
C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96				
	52.5x52.5[6]						416, 104			
D2104	47.5x47.5				676, 76	572, 76				
	52.5x52.5[6]						676, 76			
A2577	52.5x52.5				448, 120	448, 96	448, 128			
H1924	45x45							208, 32		
H2104	47.5x47.5								208, 32	416, 64
H2892	55x55									416, 64	624, 96

Notes:
1. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.
2. -2LE (T_j = 0°C to 110°C). For more details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.
3. For full part number details, see DS890, UltraScale Architecture and Product Overview.
4. All packages are 1.0mm ball pitch.
5. The GTY transceiver line rate in the F1924 footprint is package limited to 16.3Gb/s. Refer to data sheet for details.
6. These 52.5x52.5mm packages have the same PCB ball footprint as the 47.5x47.5mm packages and are footprint compatible.

UltraScale+ Device Ordering Information

For valid part/package combinations,
go to DS890, *UltraScale Architecture and Product Overview:* Device-Package Combinations and Maximum I/Os Tables

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Kintex UltraScale FPGAs

	Device Name	KU025[1]	KU035	KU040	KU060	KU085	KU095	KU115
Logic Resources	System Logic Cells (K)	318	444	530	726	1,088	1,176	1,451
	CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
	CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	4,230	5,908	7,050	9,180	13,770	4,800	18,360
	Block RAM/FIFO w/ECC (36Kb each)	360	540	600	1,080	1,620	1,680	2,160
	Block RAM/FIFO (18Kb each)	720	1,080	1,200	2,160	3,240	3,360	4,320
	Total Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
	I/O DLL	24	40	40	48	56	64	64
I/O Resources	Maximum Single-Ended HP I/Os	208	416	416	520	572	650	676
	Maximum Differential HP I/O Pairs	96	192	192	240	264	288	312
	Maximum Single-Ended HR I/Os	104	104	104	104	104	52	156
	Maximum Differential HR I/O Pairs	48	48	48	48	56	24	72
Integrated IP Resources	DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
	System Monitor	1	1	1	1	2	1	2
	PCIe® Gen1/2/3	1	2	3	3	4	4	6
	Interlaken	0	0	0	0	0	2	0
	100G Ethernet	0	0	0	0	0	2	0
	16.3Gb/s Transceivers (GTH/GTY)	12	16	20	32	56	64[2]	64
Speed Grades	Commercial	-1	-1	-1	-1	-1	-1	-1
	Extended	-2	-2 -3	-2 -3	-2 -3	-2 -3	-2	-2 -3
	Industrial	-1 -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -2	-1 -1L -2

Package Footprint[3, 4, 5, 6]	Package Dimensions (mm)	HR I/O, HP I/O, GTH/GTY						
A784[7]	23x23[8]		104, 364, 8	104, 364, 8				
A676[7]	27x27		104, 208, 16	104, 208, 16				
A900[7]	31x31		104, 364, 16	104, 364, 16				
A1156	35x35	104, 208, 12	104, 416, 16	104, 416, 20	104, 416, 28		52, 468, 28	
A1517	40x40				104, 520, 32	104, 520, 48		104, 520, 48
C1517	40x40						52, 468, 40	
D1517	40x40							104, 234, 64
B1760	42.5x42.5					104, 572, 44	52, 650, 48	104, 598, 52
A2104	47.5x47.5							156, 676, 52
B2104	47.5x47.5						52, 650, 64	104, 598, 64
D1924	45x45							156, 676, 52
F1924	45x45					104, 520, 56		104, 624, 64

Footprint Compatible with Virtex® UltraScale Devices

Notes:
1. Certain advanced configuration features are not supported in the KU025. Refer to the Configuring FPGAs section in DS890, *UltraScale Architecture and Product Overview*.
2. GTY transceivers in KU095 devices support data rates up to 16.3Gb/s.
3. Packages with the same package footprint designator, e.g., A2104, are footprint compatible with all other UltraScale devices with the same sequence. See the migration table for details on inter-family migration.
4. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
5. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.
6. See UG575, *UltraScale Architecture Packaging and Pinouts User Guide* for more information.
7. GTH transceivers in A784, A676, and A900 packages support data rates up to 12.5Gb/s.
8. 0.8mm ball pitch. All other packages listed 1mm ball pitch.

Virtex UltraScale FPGAs

	Device Name	XCVU065	XCVU080	XCVU095	XCVU125	XCVU160	XCVU190	XCVU440
Logic Resources	System Logic Cells (K)	783	975	1,176	1,567	2,027	2,350	5,541
	CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
	CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Memory Resources	Maximum Distributed RAM (Kb)	4,830	3,980	4,800	9,660	12,690	14,490	28,710
	Block RAM/FIFO w/ECC (36Kb each)	1,260	1,421	1,728	2,520	3,276	3,780	2,520
	Block RAM/FIFO (18Kb each)	2,520	2,842	3,456	5,040	6,552	7,560	5,040
	Total Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
	I/O DLL	40	64	64	80	120	120	120
	Transceiver Fractional PLL	5	8	8	10	13	15	0
I/O Resources	Maximum Single-Ended HP I/Os	468	780	780	780	650	650	1,404
	Maximum Differential HP I/O Pairs	216	360	360	360	300	300	648
	Maximum Single-Ended HR I/Os	52	52	52	52	52	52	52
	Maximum Differential HR I/O Pairs	24	24	24	24	24	24	24
Integrated IP Resources	DSP Slices	600	672	768	1,200	1,560	1,800	2,880
	System Monitor	1	1	1	2	3	3	3
	PCIe® Gen1/2/3	2	4	4	4	4	6	6
	Interlaken	3	6	6	6	8	9	0
	100G Ethernet	3	4	4	6	9	9	3
	GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
	GTY 30.5Gb/s Transceivers	20	32	32	40	52	60	0
Speed Grades	Commercial	–	–	–	–	–	–	-1
	Extended	-1H -2 -3	-1H -2 -3	-1H -2 -3	-1H -2 -3	-1H -2 -3	-1H -2 -3	-2 -3
	Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2

	Package Footprint[1, 2, 3]	Package Dimensions (mm)	HR I/O, HP I/O, GTH 16.3Gb/s, GTY 30.5Gb/s						
Footprint Compatible with Kintex® UltraScale Devices	C1517	40x40	52, 468, 20, 20	52, 468, 20, 20	52, 468, 20, 20				
	D1517	40x40		52, 286, 32, 32	52, 286, 32, 32	52, 286, 40, 32			
	B1760	42.5x42.5		52, 650, 32, 16	52, 650, 32, 16	52, 650, 36, 16			
	A2104	47.5x47.5		52, 780, 28, 24	52, 780, 28, 24	52, 780, 28, 24			
	B2104	47.5x47.5		52, 650, 32, 32	52, 650, 32, 32	52, 650, 40, 36	52, 650, 40, 36	52, 650, 40, 36	
	C2104	47.5x47.5			52, 364, 32, 32	52, 364, 40, 40	52, 364, 52, 52	52, 364, 52, 52	
	B2377	50x50							52, 1248, 36, 0
	A2577	52.5x52.5						0, 448, 60, 60	
	A2892	55x55							52, 1404, 48, 0

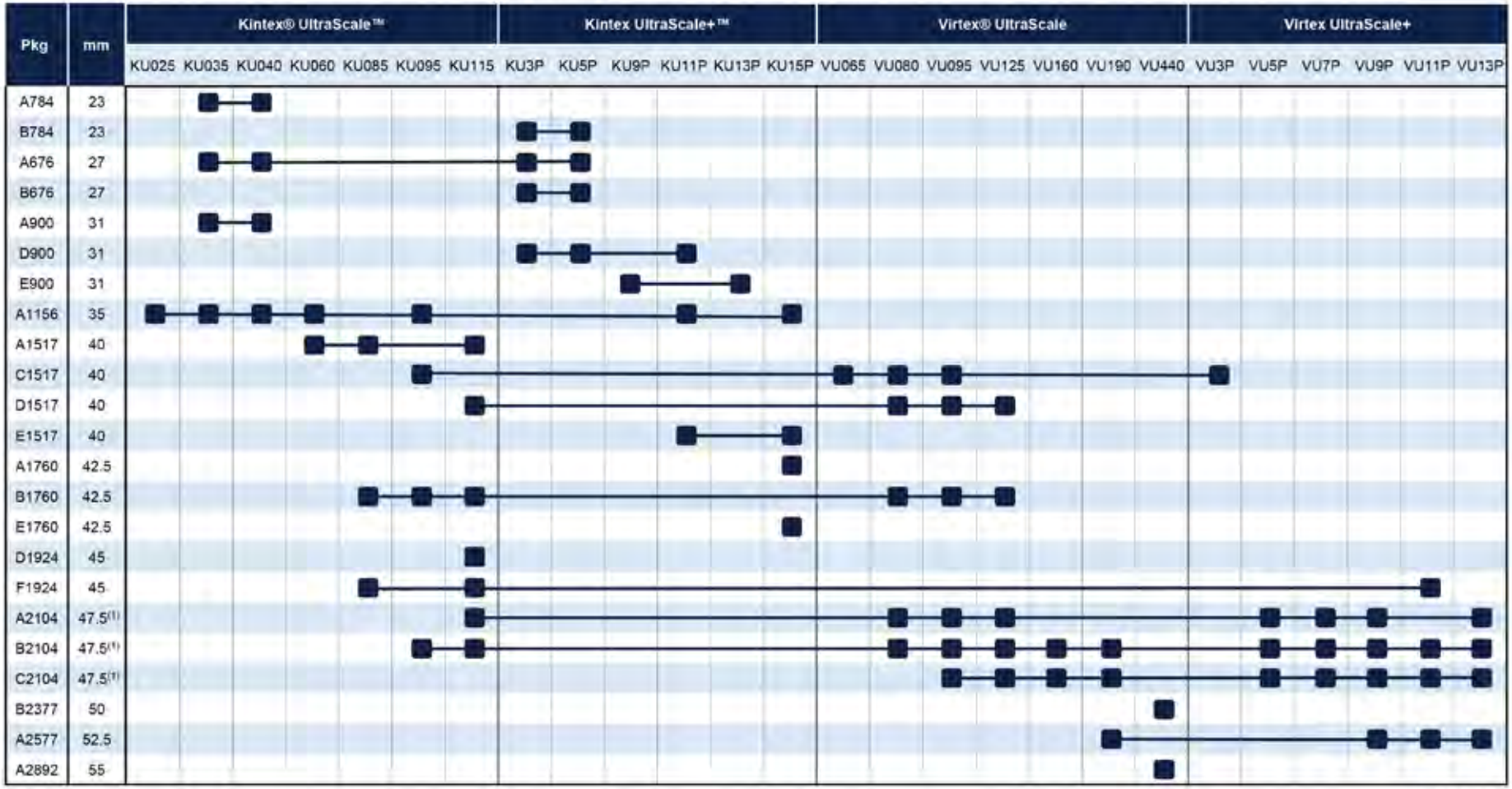
Notes:
1. Packages with the same package footprint designator, e.g., A2104, are footprint compatible with all other UltraScale devices with the same sequence. See the migration table for details on inter-family migration.
2. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.
3. See UG575, *Kintex UltraScale and Virtex UltraScale FPGAs Packaging and Pinouts User Guide* for more information.

UltraScale Device Ordering Information

For valid part/package combinations,
go to DS890, *UltraScale Architecture and Product Overview:* Device-Package Combinations and Maximum I/Os Tables

UltraScale Architecture Migration Table

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible.



Notes:

1. The body size of the VU13P device in the A2104, B2104, and C2104 packages is 52.5mm. These packages are footprint compatible with the corresponding 47.5mm body size packages. See UG583, *UltraScale Architecture PCB Design User Guide* for important migration details.

Legend

- **Device**
- **Migration Path**

Spartan-7 FPGAs

Spartan®-7 FPGAs
I/O Optimization at the Lowest Cost and Highest Performance-per-Watt

	Part Number	XC7S6	XC7S15	XC7S25	XC7S50	XC7S75	XC7S100
Logic Resources	Logic Cells	6,000	12,800	23,360	52,160	76,800	102,400
	Slices	938	2,000	3,650	8,150	12,000	16,000
	CLB Flip-Flops	7,500	16,000	29,200	65,200	96,000	128,000
Memory Resources	Max. Distributed RAM (Kb)	70	150	313	600	832	1,100
	Block RAM/FIFO w/ ECC (36 Kb each)	5	10	45	75	90	120
	Total Block RAM (Kb)	180	360	1,620	2,700	3,240	4,320
Clock Resources	Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	2	3	5	8	8
I/O Resources	Max. Single-Ended I/O Pins	100	100	150	250	400	400
	Max. Differential I/O Pairs	48	48	72	120	192	192
Embedded Hard IP Resources	DSP Slices	10	20	80	120	140	160
	Analog Mixed Signal (AMS) / XADC	0	0	1	1	1	1
	Configuration AES / HMAC Blocks	0	0	1	1	1	1
Speed Grades	Commercial Temp (C)	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
	Industrial Temp (I)	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L
	Expanded Temp (Q)	-1	-1	-1	-1	-1	-1

Package[1]	Body Area (mm)	Available User I/O: 3.3V SelectIO™ HR I/O					
CPGA196	8x8	100	100				
CSGA225	13x13	100	100	150			
CSGA324	15x15			150	210		
FTGB196	15x15	100	100	100	100		
FGGA484	23x23				250	338	338
FGGA676	27x27					400	400

Notes:
1. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other Spartan-7 devices with the same sequence. The footprint compatible devices within this family are outlined.

Artix-7 FPGAs

Artix®-7 FPGAs
Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth
(1.0V, 0.95V, 0.9V)

	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135	365
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs	72	120	72	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240	740
	PCIe® Gen2[1]	1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	2	4	4	4	4	8	8	16
Speed Grades	Commercial Temp (C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L

	Package[3], [4]	Dimensions (mm)	Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ HR I/O (GTP Transceivers)							
	CPG236	10 x 10	0.5	106 (2)	106 (2)	106 (4)	106 (2)	106 (2)			
	CSG324	15 x 15	0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)	
	CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)			
	FTG256	17 x 17	1.0		170 (0)		170 (0)	170 (0)	170 (0)	170 (0)	
	SBG484	19 x 19	0.8								285 (4)
Footprint Compatible	FGG484[5]	23 x 23	1.0		250 (4)		250 (4)	250 (4)	285 (4)	285 (4)	
Footprint Compatible	FBG484[5]	23 x 23	1.0								285 (4)
	FGG676[6]	27 x 27	1.0						300 (8)	300 (8)	
	FBG676[6]	27 x 27	1.0								400 (8)
	FFG1156	35 x 35	1.0								500 (16)

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Leaded package option available for all packages. See DS180, *7 Series FPGAs Overview* for package details.
4. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.
5. Devices in FGG484 and FBG484 are footprint compatible.
6. Devices in FGG676 and FBG676 are footprint compatible.

Kintex-7 FPGAs

			Optimized for Best Price-Performance (1.0V, 0.95V, 0.9V)						
	Part Number		XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	EasyPath™ Cost Reduction Solutions[1]		—	—	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices		10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells		65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops		82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kb)		838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)		135	325	445	715	795	835	955
	Total Block RAM (Kb)		4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)		6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O		300	400	500	300	500	400	400
	Maximum Differential I/O Pairs		144	192	240	144	240	192	192
Integrated IP Resources	DSP48 Slices		240	600	840	1,440	1,540	1,680	1,920
	PCIe® Gen2[2]		1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)		8	8	16	24	16	32	32
Speed Grades	Commercial Temp (C)		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)		-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)		-1, -2	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L
	Package[3]	Dimensions (mm)	**Available User I/O:** 3.3V HR I/O, 1.8V HP I/Os (GTX)						
	FBG484[4]	23 x 23	185, 100 (4)	185, 100 (4)					
Footprint Compatible	FBG676[4]	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)		250, 150 (8)		
	FFG676	27 x 27		250, 150 (8)	250, 150 (8)		250, 150 (8)		
Footprint Compatible	FBG900[4]	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG900	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG901	31 x 31				300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156	35 x 35						400, 0 (32)	400, 0 (32)

Notes:
1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. See DS180, *7 Series FPGAs Overview*, for package details.
4. GTX transceivers in FB packages support the following maximum data rates: 10.3Gb/s in FBG484; 6.6Gb/s in FBG676 and FBG900. See DS182, *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics*, for details.

Virtex-7 FPGAs

		Optimized for Highest System Performance and Capacity (1.0V)										
	Part Number	XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	XC7VH580T	XC7VH870T
	EasyPath™ Cost Reduction Solutions[1]	XCE7V585T	—	XCE7VX330T	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCE7VX980T	—	—	—
Logic Resources	Slices	91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells	582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160
	CLB Flip-Flops	728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)	6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Block RAM/FIFO w/ ECC (36 Kb each)	795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410
	Total Block RAM (Kb)	28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
Clocking	CMTs (1 MMCM + 1 PLL)	18	24	14	12	14	20	20	18	24	12	18
I/O Resources	Maximum Single-Ended I/O	850	1,200	700	600	700	600	1,000	900	1,100	600	300
	Maximum Differential I/O Pairs	408	576	336	288	336	288	480	432	528	288	144
	DSP Slices	1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCIe® Gen2[2]	3	4	—	—	4	—	—	—	—	—	—
	PCIe Gen3	—	—	2	2	—	2	3	3	4	2	3
Integrated IP Resources	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)[3]	36	36	—	—	56	—	—	—	—	—	—
	GTH Transceivers (13.1 Gb/s Max Rate)[4]	—	—	28	48	—	80	80	72	96	48	72
	GTZ Transceivers (28.05 Gb/s Max Rate)	—	—	—	—	—	—	—	—	—	8	16
Speed Grades	Commercial Temp (C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)[5]	-2L, -3	-2L, -2G	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L	-2L, -2G	-2L, -2G	-2L, -2G
	Industrial Temp (I)	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	—	—

	Package[6]	Dimensions (mm)	Available User I/O: 3.3V HR I/O, 1.8V HP I/Os (GTX, GTH)									1.8V HP I/O (GTH, GTZ)
	FFG1157[7]	35 x 35	0, 600 (20, 0)	0, 600 (20, 0)	0, 600 (0, 20)	0, 600 (20, 0)			0, 600 (0, 20)			
Footprint Compatible	FFG1761[7]	42.5 x 42.5	100, 750 (36, 0)	50, 650 (0, 28)		0, 700 (28, 0)			0, 850 (0, 36)			
	FHG1761	45 x 45	0, 850 (36, 0)									
	FLG1925	45 x 45	0, 1200 (16, 0)									
	FFG1158[7]	35 x 35			0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)		0, 350 (0, 48)			
Footprint Compatible	FFG1926	45 x 45							0, 720 (0, 64)	0, 720 (0, 64)		
	FLG1926	45 x 45								0, 720 (0, 64)		
	FFG1927[7]	45 x 45			0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)		0, 600 (0, 80)			
Footprint Compatible	FFG1928	45 x 45								0, 480 (0, 72)		
	FLG1928	45 x 45									0, 480 (0, 96)	
Footprint Compatible	FFG1930	45 x 45				0, 700 (24, 0)			0, 1000 (0, 24)	0, 900 (0, 24)		
	FLG1930	45 x 45									0, 1100 (0, 24)	
	FLG1155	35 x 35										400 (24, 8)
	FLG1931	45 x 45										600 (48, 8)
	FLG1932	45 x 45										300 (72, 16)

Notes:
1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. 12.5 Gb/s support in "-3E", "-2GE" speed/temperature grade; 10.3125 Gb/s support in "2C", "-2LE", and "-2I" speed grade.
4. 13.1 Gb/s support in "-3E", "-2GE" speed grade; 11.3 Gb/s support in "2C" , "-2LE" and "-2I" speed/temperature grades.
5. -2G only applies to Stacked Silicon Interconnect devices and supports 12.5G GTX, 13.1G GTH, 28.05G GTZ with -2 fabric.
6. Leaded package options ("FFxxxx"/"FLxxxx"/"FHxxxx") available for all packages. "HCxxxx" is not offered in a leaded option.
7. See DS180, *7 Series FPGAs Overview* for package details.

7 Series Device Ordering Information

SPARTAN-7

XC	7	S	###	-1	FG	G	A	484	C
Commercial Xilinx	Generation	Family	Logic Cells In 1K units	Speed Grade -1 = Slowest -L1 = Low Power -2 = Mid	Package Type CP: Wire-bond (.5mm) CS: Wire-bond (.8mm) FG: Wire-bond (1mm) FT: Wire-bond (1mm)	G: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (C, I, Q)

ARTIX-7

XC	7	A	###	-1	FB	G	484	C
Xilinx Commercial	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Slowest -L1 = Low Power -L2 = Low Power -2 = Mid -3 = Highest	Package Type CP: Wire-bond (.5 mm) CS: Wire-bond (.8 mm) FB: Lidless Flip-Chip (1 mm) FF: Flip-Chip (1 mm) FG: Wire-bond (1 mm) FT: Wire-bond (1 mm) SB: Lidless Flip-Chip (.8 mm)	V: RoHS 6/6 G: RoHS 6/6 w/Exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

KINTEX-7

XC	7	K	###	-1	FF	G	900	C
Xilinx Commercial	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Slowest -L2 = Low Power -2 = Mid -3 = Highest	Package Type FB: Lidless Flip-Chip (1 mm) FF: Flip-Chip (1 mm)	V: RoHS 6/6 G: RoHS 6/6 w/Exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

VIRTEX-7

XC	7	V	###	-1	FF	G	1156	C
Xilinx Commercial	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Slowest -2 = Mid -L2 = Low Power -3 = Highest	Package Type FF: Flip-Chip (1 mm) FH: Flip-Chip (1 mm) FL: Flip-Chip (1 mm) HC: Ceramic Flip-Chip (1 mm)	V: RoHS 6/6 G: RoHS 6/6 w/Exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

Notes:
-L1 is the ordering code for the lower power, -1L speed grade.
-L2 is the ordering code for the lower power, -2L speed grade.

C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = –40°C to +100°C) Q = Expanded (Tj = –40°C to +125°C)

Spartan-6 FPGAs

	Spartan®-6 LX FPGAs I/O Optimization at the Lowest Cost (1.2V, 1.0V)								Spartan-6 LXT FPGAs I/O Optimization at the Lowest-Cost with Serial Connectivity (1.2V)				
Part Number	XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX75	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
Slices[1]	600	1,430	2,278	3,758	6,822	11,662	15,822	23,038	3,758	6,822	11,662	15,822	23,038
Logic Cells[2]	3,840	9,152	14,579	24,051	43,661	74,637	101,261	147,443	24,051	43,661	74,637	101,261	147,443
CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	184,304	30,064	54,576	93,296	126,576	184,304
Max. Distributed RAM (Kb)	75	90	136	229	401	692	976	1,355	229	401	692	976	1,355
Block RAM (18Kb each)	12	32	32	52	116	172	268	268	52	116	172	268	268
Total Block RAM (Kb)[3]	216	576	576	936	2,088	3,096	4,824	4,824	936	2,088	3,096	4,824	4,824
Clock Mgmt Tiles (CMT)[4]	2	2	2	2	4	6	6	6	2	4	6	6	6
Max. Single-Ended I/O Pins	132	200	232	266	358	408	480	576	250	296	348	498	540
Max. Differential I/O Pairs	66	100	116	133	179	204	240	288	125	148	174	249	270
DSP48A1 Slices[5]	8	16	32	38	58	132	180	180	38	58	132	180	180
Endpoint Block for PCIe®	—	—	—	—	—	—	—	—	1	1	1	1	1
Memory Controller Blocks	0	2	2	2	2	4	4	4	2	2	4	4	4
GTP Low-Power Transceivers	—	—	—	—	—	—	—	—	2	4	8	8	8
Commercial Speed Grade[10]	-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
Industrial Speed Grade[10]	-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
Configuration Memory (Mb)	2.7	2.7	3.7	6.4	11.9	19.6	26.5	33.8	6.4	11.9	19.6	26.5	33.8
Package	Body Area (mm)	Ball Pitch (mm)	**Maximum User I/O**: SelectIO™ Interface Pins (GTP Transceivers)[6]										
CPG196[7]	8 x 8	0.5	106	106	106								
TQG144[7]	20 x 20	0.5	102	102									
CSG225[8]	13 x 13	0.8	132	160	160								
CSG324	15 x 15	0.8		200	232	226	218			190 (2)	190 (4)		
CSG484[9]	19 x 19	0.8					320	328	338	338		296 (4)	292 (4)	296 (4)	296 (4)
FT(G)256	17 x 17	1.0		186	186	186							
FG(G)484[9]	23 x 23	1.0				266	316	280	326	338	250 (2)	296 (4)	268 (4)	296 (4)	296 (4)
FG(G)676	27 x 27	1.0					358	408	480	498			348 (8)	376 (8)	396 (8)
FG(G)900	31 x 31	1.0								576				498 (8)	540 (8)

Notes:
1. Each slice contains four LUTs and eight flip-flops.
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
3. Block RAM are fundamentally 18Kb in size. Each block can also be used as two independent 9 Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.
6. The LX device pinouts are not compatible with the LXT device pinouts.
7. CPG196 and TQG144 do not have memory controller support. -3N is not available for these packages.
8. CSG225 has X8 memory controller support in the LX9 and LX16 devices. There is no memory controller in the LX4 devices.
9. Devices in the FG(G)484 and CSG484 packages have support for two memory controllers.
10. Devices with -3N speed grade do not support MCB functionality.

Spartan-6 Device Ordering Information

Footprint

XC	6	S	LX LXT	###	-1	FG	G	900	C
Xilinx Commercial	Generation	Family	Sub-families	Logic Cells In 1K units	Speed Grade -L1 = Low Power -2 = Mid -3 = Highest	Package Type CP: Wire-bond (.5mm) TQ: Quad Flat Pack (.5mm) CS: Wire-bond (.8mm) FT: Wire-bond (1mm) FG: Wire-bond (1mm)	G: RoHS 6/6	Package Pin Count	Temperature Grade (C, E, I)

Notes:
-L1 is the ordering code for the lower power, -1L speed grade.
-L2 is the ordering code for the lower power, -2L speed grade.

C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = –40°C to +100°C)

For valid part/package combinations,
go to DS160, *Spartan-6 Family Overview*: Device-Package Combinations and Maximum I/Os Tables

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

XA Zynq UltraScale+ MPSoCs

		Device Name[1]	ZU2EG	ZU3EG	ZU4EV	ZU5EV
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.2GHz			
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB			
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore up to 500MHz			
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core			
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 600MHz			
		Memory	L2 Cache 64KB			
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC			
		Static Memory Interfaces	NAND, 2x Quad-SPI			
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet			
		General Connectivity	2xUSB 2.0, 2x SD/SDIO/eMMC, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains			
		Security	RSA, AES, and SHA			
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor			
PS to PL Interface			12 x 32/64/128b AXI Ports			
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256
		CLB Flip-Flops (K)	94	141	176	234
		CLB LUTs (K)	47	71	88	117
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1
		UltraRAM (Mb)	-	-	14.0	18.0
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4
	Integrated IP	DSP Slices	240	360	728	1,248
		VCU	-	-	1	1
		PCI Express Gen 3x16 / Gen4x8	-	-	2	2
		150G Interlaken	-	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-
		AMS - System Monitor	1	1	1	1
	Transceivers	GTH 12.5Gb/s Transceivers	-	-	16	16
	Speed Grades	I-Grade	-1 (0.85V), -L1 (0.72V)			
		Q-Grade	-1 (0.85V)			

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

XA Zynq UltraScale+ MPSoCs

PS I/Os(1), 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os
PS-GTR 6Gb/s, GTH 12.5Gb/s

Pkg Footprint(2)	Dimensions (mm)	XAZU2EG	XAZU3EG	XAZU4EV	XAZU5EV
SBVA484(3)	19x19	170, 24, 58 4, 0	170, 24, 58 4, 0		
SFVA625(3)	21x21	170, 24, 156 4, 0	170, 24, 156 4, 0		
SFVC784(3)	23x23	214, 96, 156 4, 0	214, 96, 156 4, 0	214, 96, 156 4, 4	214, 96, 156 4, 4

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
3. These packages are only offered in 0.8mm ballpitch.

XA Zynq-7000 SoCs

		Device Name[1]	XA7Z010	XA7Z020	XA7Z030
Processing System (PS)	Application Processor Unit	Processor Core	**Dual** ARM® Cortex™-A9 MPCore™ up to 667MHz		
		Processor Extension	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per Processor		
	Memory	L1 Cache	32KB I / D per Core		
		L2 Cache	512KB		
		On-Chip Memory	256KB		
	External Memory	Dynamic Memory Interface	x32/x64: DDR3, DDR3L, DDR2, LPDDR2		
		Static Memory Interfaces	NAND, NOR, 2x Quad-SPI		
	Connectivity	High-Speed Connectivity	2x Tri-mode Gigabit Ethernet		
		General Connectivity	2xUSB 2.0, 2x SD/SDIO/eMMC, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Integrated Block Functionality	Security	RSA, AES, and SHA		
		AMS - System Monitor	2x12-bit, 1MSPS - Temperature, Voltage, and Current Monitor		
PS to PL Interface			9 x 32/64 AXI Ports		
Programmable Logic (PL)		Xilinx 7 Series PL Equivalent	Artix-7	Artix-7	Kintex-7
	Programmable Functionality	Logic Cells	28,160	85,280	125,760
		CLB Flip-Flops	35,300	106,400	157,200
		CLB LUTs	17,600	53,300	78,600
	Memory	Total Block RAM (KB)	240	560	1,060
		(# 36 Kb Blocks)	(60)	(140)	(265)
	Integrated IP	DSP Slices	80	220	400
		Peak DSP Performance	100 GMACs	276 GMACs	593 GMACs
		PCI Express	-	-	Gen2 x4
		AMS / XADC	AES and SHA 256b Decryption and Authentication for Secure Programmable Configuration		
	Speed Grades	I-Grade	-1		
		Q-Grade	-1		
	Package[1]	Size (mm) / Pitch (mm)	HR I/O[2], HP I/O[3], PS I/O[4], GTX Transceiver		
Package	CLG225	13x13 / 0.8	54, 0, 84, 0		
	CLG400	17x17 / 0.8	100, 0, 128, 0	125, 0, 128, 0	
	CLG484	19x19 / 0.8		200, 0, 128, 0	
	FBV484	23x23 / 1.0			100, 63, 128, 4

Notes:
1. All packages listed are Pb-free.
2. HR = High Range I/O with support for I/O voltage from 1.2V up to 3.3V.
3. HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.
4. PS I/O includes user I/O and DDR I/O.

XA Artix-7 FPGAs

Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)

	Part Number	XA7A12T	XA7A15T	XA7A25T	XA7A35T	XA7A50T	XA7A75T	XA7A100T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	285	285
	Maximum Differential I/O Pairs	72	120	72	120	120	137	137
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240
	PCIe® Gen2[1]	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTP Transceivers (6.25Gb/s Max Rate)[2]	2	4	4	4	4	4	4
Speed Grades	I-Grade	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Q-Grade	-1	-1	-1	-1	-1	-1	-1

Package[3]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)						
CPG236	10 x 10	0.5	106 (2)	106 (2)	106 (4)	106 (2)	106 (2)		
CSG324	15 x 15	0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)
CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)		
FGG484	23 x 23	1.0		250 (4)		250 (4)	250 (4)	285 (4)	285 (4)

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the CSG324 devices are available without transceivers. See the Package section of this table for details.
3. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.

XA Spartan-7 FPGAs

			I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V)					
		Part Number	XA7S6	XA7S15	XA7S25	XA7S50	XA7S75	XA7S100
		Logic Cells	6,000	12,800	23,360	52,160	76,800	102,400
		Slices	938	2,000	3,650	8,151	12,000	16,000
		CLB Flip-Flops	7,500	16,000	29,200	65,200	96,000	128,000
		Max. Distributed RAM (Kb)	70	150	313	600	832	1,100
		Block RAM/FIFO w/ ECC (36Kb each)	5	10	45	75	90	120
		Total Block RAM (Kb)	180	360	1,620	2,700	3,240	4,320
		Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	2	3	5	8	8
		Max. Single-Ended I/O Pins	100	100	150	250	400	400
		Max. Differential I/O Pairs	48	48	72	120	192	192
		DSP Slices	10	20	80	120	140	160
		Analog Mixed Signal (AMS) / XADC	0	0	1	1	1	1
		Configuration AES / HMAC Blocks	0	0	1	1	1	1
		I-Grade	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
		Q-Grade	-1	-1	-1	-1	-1	-1
Package	Dimensions (mm)	Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ HR I/O					
CPGA196	8x8	0.5	100	100				
CSGA225	13x13	0.8	100	100	150			
CSGA324	15x15	0.8			150	210		
FTGB196	15x15	1.0	100	100	100	100		
FGGA484	23x23	1.0				250	338	338
FGGA676	27x27	1.0					400	400

XA Spartan-6 FPGAs

Transceiver Optimization at the Lowest Cost
(1.2V)

	Part Number	XA6SLX4	XA6SLX9	XA6SLX16	XA6SLX25	XA6SLX45	XA6SLX75	XA6SLX100	XA6SLX25T	XA6SLX45T	XA6SLX75T
Logic Resources	Logic Cells	3,840	9,152	14,579	24,051	43,661	74,637	101,262	24,051	43,661	74,637
	Slices	600	1,430	2,278	3,758	6,822	11,662	15,822	3,758	6,822	11,662
	CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	30,064	54,576	93,296
Memory Resources	Maximum Distributed RAM (Kb)	75	90	136	229	401	692	976	229	401	692
	Block RAM (18Kb ea.)	12	32	32	52	116	172	268	52	116	172
	Total Block RAM (Kb)	216	576	576	936	2,088	3,096	4,824	936	2,088	3,096
Clock Resources	CMTs (2 DCM + 1 PLL)	2	2	2	2	4	6	6	2	4	6
Embedded Hard IP Resources	Memory Controller Blocks (Max)	0	2	2	2	2	2	2	2	2	2
	Endpoint Blocks PCIe®	0	0	0	0	0	0	0	1	1	1
	GTP Transceivers (3.2Gb/s Max Rate)	0	0	0	0	0	0	0	2	4	4
	Total I/O Banks	4	4	4	4	4	4	4	4	4	4
	Max User I/O	132	200	232	266	320	328	326	250	296	268
Speed Grades	I-Grade						-2, -3				
	Q-Grade						-2, -3				

Package	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)									
CSG225	13 x 13	0.8	132 (0)	160 (0)	160 (0)							
FTG256	17 x 17	1.0		186 (0)	186 (0)	186 (0)						
CSG324	15 x 15	0.8		200 (0)	232 (0)	226 (0)	218 (0)			190 (2)	190 (4)	
CSG484	19 x 19	0.8					320 (0)	328 (0)				
FGG484	23 x 23	1.0				266 (0)	316 (0)	280 (0)	326 (0)	250 (2)	296 (4)	268 (4)

XA Device Ordering Information

ZYNQ UltraSCALE+

XA	ZU	#	E	G	-1	S	B	V	A	484	I
Xilinx Automotive	Generation	Value Index	Processor System E: Dual RPU Quad APU Single GPU	Engine Type G: General Purpose V: Video	Speed Grade -1 = Standard -1L = Low Power	S: Flip-Chip (.8mm)	F: Lid B: Lidless	V: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (I, Q)

ZYNQ

XA	7	Z	###	-1	FB	V	484	Q
Xilinx Automotive	Generation	Family	Value Index	Speed Grade -1 = Standard	CL: Wire-bond (.8 mm) FB: Flip-Chip (1 mm)	V: RoHS 6/6 G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

SPARTAN 7

XA	7	S	###	-1	FG	G	A	484	Q
Xilinx Automotive	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Standard -2 = Medium	CP: Wire-bond (.5 mm) FT: Wire-bond (1mm) CS: Wire-bond (.8 mm) FG: Wire-bond (1 mm)	G: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (I, Q)

ARTIX 7

XA	7	A	###	-1	CP	G	236	I
Xilinx Automotive	Generation	Family	Logic Cells in 1K units	Speed Grade -1 = Standard -2 = Medium	CP: Wire-bond (.5mm) CS: Wire-bond (.8mm) FG: Wire-bond (1mm)	G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

SPARTAN 6

XA	6	S	LX LXT	###	-1	FG	G	484	Q
Xilinx Automotive	Generation	Family	Sub-families LX: Logic LXT: Logic + Transceivers	Logic Cells in 1K Units	Speed Grade -2 = Mid -3 = Highest	CS: Wire-bond (.8 mm) FT: Wire-bond (1mm) FG: Wire-bond (1 mm)	G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

I = Tj from –40°C to +100°C ; Q = Tj from –40°C to +125°C

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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